



US

University of Sussex



MEMS Fabrication of Silicon Ion Trap Arrays



DTO

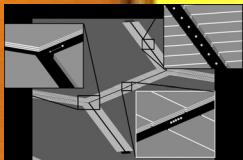
W. K. Hensinger^{1,2}, D. Stick¹, J. Sterk¹, M. Madsen¹, W. Noonan³, M. Pedersen³, S. Gross³, and M. Huff³ and C. Monroe¹

¹ FOCUS Center and Department of Physics, University of Michigan, Ann Arbor, Michigan 48109

² Department of Physics and Astronomy, University of Sussex, Falmer, Brighton, East Sussex, BN1 9QH, UK

³ MEMS and Nanotechnology Exchange, Reston, Virginia 20191-5434

Scaling up ion trap quantum computing

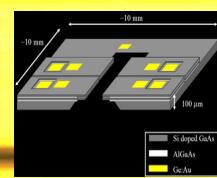


Multi-zone arrays with memory (storage) and interaction (entanglement) regions.

Integrated chip traps:



Integrated Gallium Arsenide ion trap chip successfully operated. Multiple layers of GaAs, Al_{0.7}Ga_{0.3}As, grown via molecular beam epitaxy.



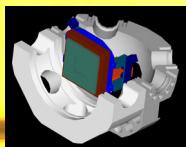
Cantilevers and bondpads are formed via photolithography, reactive ion and wet etches.



Ion trapped, but shallow trap (only 0.08 eV)

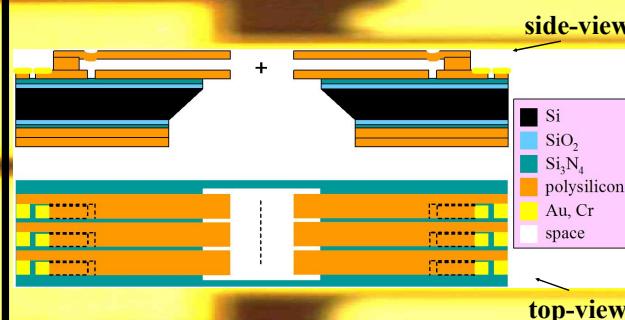
See: Ion trap in a Semiconductor Chip, D. Stick, W. K. Hensinger, S. Olmschenk, M. J. Madsen, K. Schwab and C. Monroe, Nature Physics 2, 36 (2006)

Fast turn-around time ion trap testing system for efficient testing of new MEMS ion chip traps.

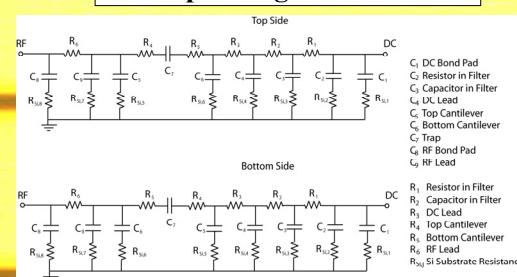


Second Generation Silicon MEMS devices

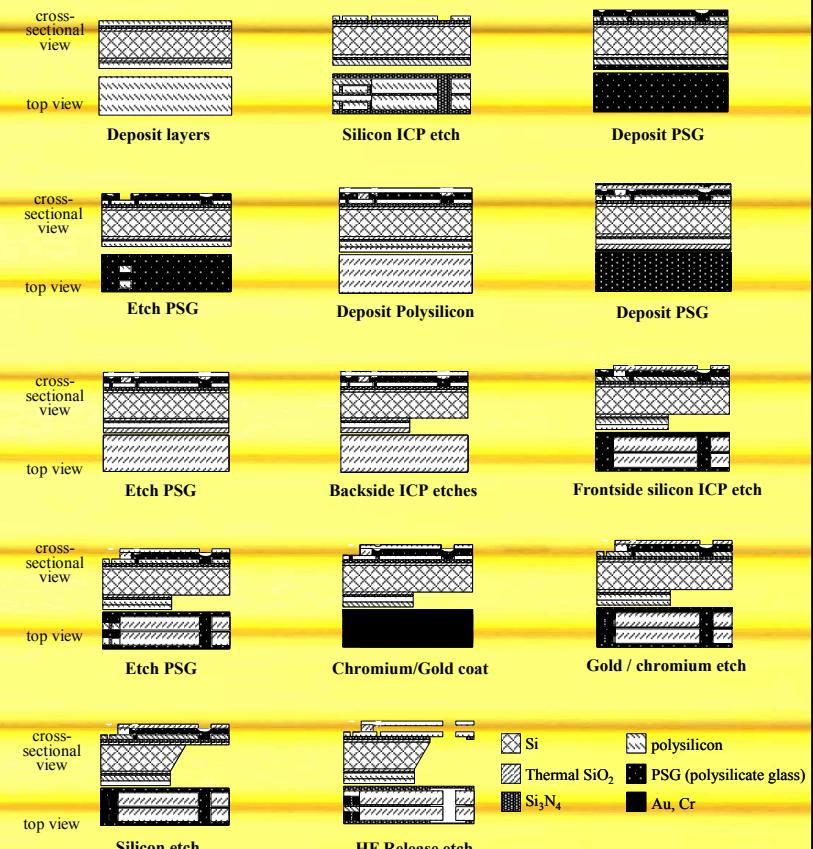
- Need capability to apply larger voltages (so far: 10V rf max. at 16MHz)
- Need to reduce RF losses in insulator material
- Need to reduce heat dissipation



Corresponding electric circuit



The process sequence



Current status

- Test run is currently carried out
- Test final structures in the next 6 months